CLAIMS

What is claimed is:

1. A method of converting a first network representation adapted for use in a programmable logic device into a second network representation, wherein the first network representation describes an input node connected to a first destination circuit via a first signal path and connected to a second destination circuit via a second signal path, the method comprising:
    1. inserting a first macro in the first signal path, the first macro including a first delay-element representation and a first stopper-cell representation;
    2. inserting a second macro in the second signal path, the second macro including a second delay-element representation and a second stopper-cell representation;
    3. simulating a first signal traversing the first signal path and a second signal traversing the second signal path;
    4. logging a first simulated delay for signals traversing the first signal path;
    5. logging a second simulated delay for signals traversing the second signal path;
    6. comparing the first and second simulated delays to find the difference between the first and second simulated delays; and
    7. substituting the first delay-element representation with a third delay-element representation to reduce the difference between the first and second simulated delays.

2. The method of claim 1, wherein the second representation is adapted for use in a mask-programmed integrated circuit.

3. The method of claim 1, wherein the first delay-element representation defines a first circuit component and the third delay-element representation defines a second circuit component, and wherein the third circuit component induces less signal propagation delay than does the first circuit component.

4. The method of claim 1, wherein the first and second delay elements are library elements that define active semiconductor components.

5. The method of claim 1, wherein the first and second stopper cells define only inactive circuit components.

6. The method of claim 1, wherein the first delay-element representation defines at least one of a buffer and an inverter.